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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,199	09/18/2003	Ashish Kumar Goel	852463.403	7173

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EXAMINER	
CHASE, SHELLY A	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,199	GOEL ET AL.	
	Examiner	Art Unit	
	Shelly A. Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-16* is/are allowed.

6)☒ Claim(s) *1,3,7,8,17-20 and 24-32* is/are rejected.

7)☒ Claim(s) *2, 4, 5, 6, & 21-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SHELLY CHASE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7-15-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 32 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119, which papers have been placed of record in the file.

Information Disclosure Statement

3. The references listed in the information disclosure statement submitted on 7-15-2004 have been considered by the examiner (see attached PTO-1449).

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 31 and 31 have been renumbered claims 31 and 32 respectively.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **17** to **20, 23**, and **26** to **32** are rejected under 35 U.S.C. 102(e) as being anticipated by Trimberger (USP 7111224 B1).

Claim **17**:

Trimberger teaches a system for an on-chip error correction circuit to be used during the configuration of a field programmable gate array (FPGA) memory, the system comprising: an array (12) of memory cells (14) wherein each memory cell has a data input coupled to a frame register (11) with the data input for each row of the memory cell corresponding to the data in frame register (see col. 4, lines 36 to 60), which reads on "loading one of a plurality of configuration data frames into a frame register." Trimberger also teaches that an error correction code circuit (13) receives the data outputted from the frame register and checks the data for errors (see col. 4, lines 28 to 35 and col. 5, lines 15 to 30).

Trimberger further teaches that if an error was detected, the detected error is corrected and the data is loaded back into the memory cell and if no error is detected, then analyzed the next column (see col. 5, lines 35 to 45). Trimberger teaches that the steps of loading shifting and error checking process are repeated for read back data (see col. 8, lines 40 et seq.).

As per claims **18** to **20**, Trimberger teaches checking the columns in the memory cell one after the other as well as using an error correction code for the detection of errors wherein any error correction code can be used (see col. 5, lines 35 to 48).

Trimberger further teaches a control circuit for clocking and timing the configuration process (see col. 7, lines 4 et seq.).

As per claim **23, 27** and **28** Trimberger teaches a configurable FPGA (see col. 3, lines 48 to 52), a step of clearing the data shift register (22) (see col. 7, lines 31 to 34) and that the memory cell (14) can be a D flip-flop (see col. 4, lines 50 to 55).

As per claim **26**, Trimberger teaches an address module (16) with an address increment input for incrementing the stages of the address module (see col. 5, lines 63 to col. 6, line 20).

Claim **32**:

Claim **32** is similar to claim 19 except for the programmable logic device and is rejected under the same rationale applied to claim 19.

Claim **29**:

Trimberger teaches a system for an on-chip error correction circuit to be used during the configuration of a field programmable gate array (FPGA) memory, the system comprising: an array (12) of memory cells (14) wherein each memory cell has a data input coupled to a frame register (11) with the data input for each row of the memory cell corresponding to the data in frame register (see col. 4, lines 36 to 60), which reads on "loading one of a plurality of configuration data frames into a frame register." Trimberger also teaches that an error correction code circuit (ECCC) (13) receives the

data outputted from the frame register wherein the outputted data is checked for errors (see col. 4, lines 28 to 35 and col. 5, lines 15 to 30).

Trimberger further teaches that the ECCC corrects the detected error and load the data back into the memory cell (see col. 5, lines 35 to 45).

As per claims **30** and **31**, Trimberger teaches that the configuration module includes a control unit (24) that controls the operation of the module (see col. 7, lines 4 to 30) and that the system is an on-chip error correction circuit (see col. 4, lines 6 to 20).

Claim Rejections - 35 USC § 103

6. Claims **1, 3, 7** and **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger in view of Plants (USP 6560743 B2).

Claim **1**:

Trimberger teaches a system for an on-chip error correction circuit to be used during the configuration of a field programmable gate array (FPGA) memory, the system comprising: an array (12) or memory cells (14) wherein each memory cell has a data input coupled to a frame register (11) with the data input for each row of the memory cell corresponding to the data in frame register (see col. 4, lines 36 to 60), which reads on "loading one of a plurality of configuration data frames into a frame register." Trimberger also teaches that an error correction code circuit (13) receives the data outputted from the frame register checks the data for errors (see col. 4, lines 28 to 35 and col. 5, lines 15 to 30).

Trimberger further teaches that if an error was detected, the error is corrected and the data is loaded back into the memory cell and if an error is not detected, then analyzed the next column (see col. 5, lines 35 to 45). Timberger teaches that steps of loading, shifting and error checking process are repeated for read back data (see col. 8, lines 40 et seq.).

Trimberger does not specifically teach reloading the frame register of the PLD and incrementing an error counter value if errors are encountered; however, Plants in an analogous art teaches reloading the data from the EEPROM when an error is detected in the configuration data of the FPGA (see col. 7, lines 30 to 36) and using a row counter and a column counter during the error checking process where the row counter and the column counter are reset for the verification process (see col. 7, lines 1 et seq.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of checking the data of an FPGA for errors as taught by Trimberger to include reloading the data once an error is detected and using a row counter and a column counter as taught by Plants. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to include a step of reloading the data to ensue all errors are detected effectively and a step of using a counter to keep track of the process as taught by Plants (see pg. Col. lines 28 et seq.).

As per claim **3**, Trimberger teaches that the error correction code circuit (13) can apply any type of error detection code (see col. 5, lines 39 to 49).

7. Claims **7** and **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger in view of Plants, further in view of Baxter et al. (USP 5870586).

As per claims **7** and **8**, Trimberger in view of Plants does not specifically teach that the PLD operates as a master or as a slave; however, Baxter in an analogous art teaches that a FPGA can be configured in various modes such as a master mode or a slave made (see col. 4, lines 1 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the configuration of the FPGA of Trimberger in view of Plants to include configuring the FPGA in a master mode or a slave mode as taught by Baxter since, Baxter teaches that designers have more flexibility for applying different modes to a circuit design by reconfiguring the FPGA in different modes (see col. 2, lines 44 et seq.). This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a step of achieving flexibility in configuring a FPGA as taught by Baxter.

8. Claims **24** and **25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger in view of Baxter.

As per claims **24** and **25**, Trimberger does not specifically teach that the PLD is operated as a master or as a slave; however, Baxter in an analogous art teaches that a FPGA can be configured in various modes such as a master mode or a slave made (see col. 4, lines 1 et seq.). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to modify the configuration of the PFGA of Trimberger to include configuring the FPGA in a master mode or a slave mode as taught by Baxter since, Baxter teaches that designers have more flexibility for applying different modes to a circuit design by reconfiguring the FPGA in different modes (see col. 2, lines 44 et seq.). This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a step of achieving flexibility in configuring a FPGA as taught by Baxter.

Allowable Subject Matter

9. Claims 2, 4, 5, 6, 21 and 22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 9 to 16 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: the primary reason for allowance of the claims is the inclusion of the limitation "comparing means for comparing the error count to a pre-determined threshold value" that is not found in the prior art made of record. The prior art made of record teaches a method and a device for configuring a FPGA using counters as detailed above; however, the prior art made of record, taken alone or in combination fails to tech or fairly suggest or render obvious the novel element of utilizing a counter against a "pre-

determined threshold value as claimed in the independent claim. Therefore the claims are allowed over the prior art made of record.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A. Chase whose telephone number is 571-272-3816. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SHELLY CHASE
PRIMARY EXAMINER